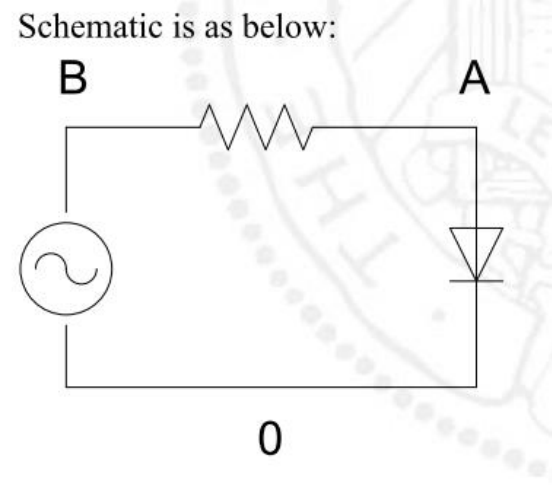
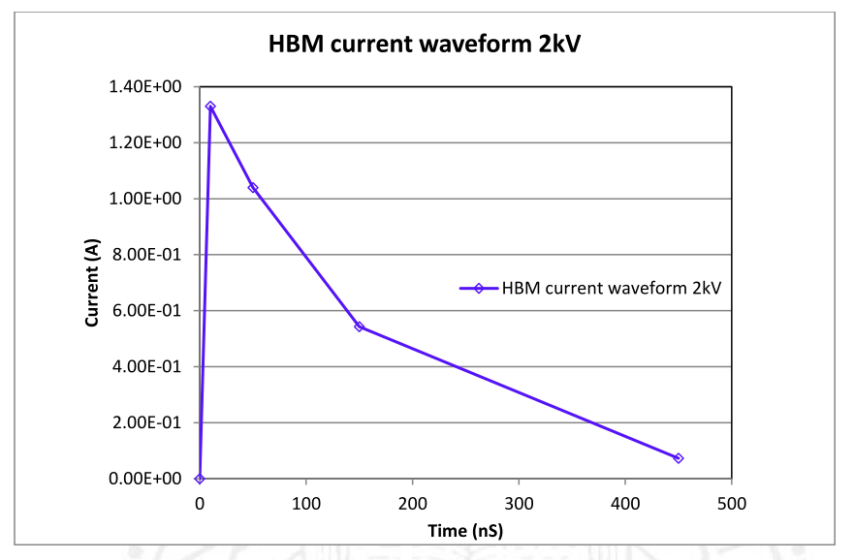
Design of Diode for Higher Voltage use cases through Manipulation of STI and N+, P+ Diffusion Wells

Joseph Gozum & Martin Liu

Human Body Model

In our experimentation, we utilized the standard Human Body Model at 2kV to test/verify our results.





Manipulation of Depth of STI

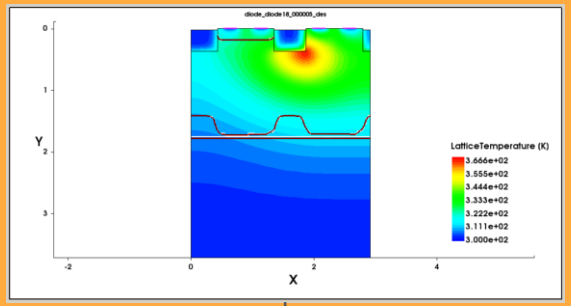
Depth

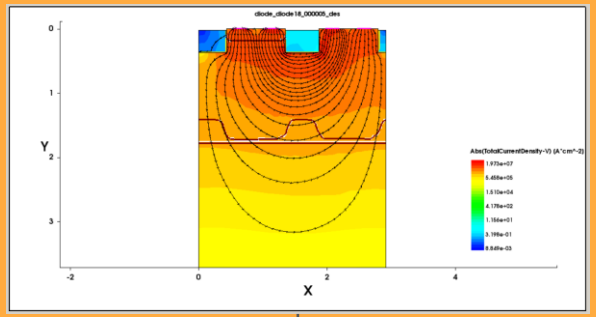
- Lattice Temperature
- Hotspots
- Current Streamlines

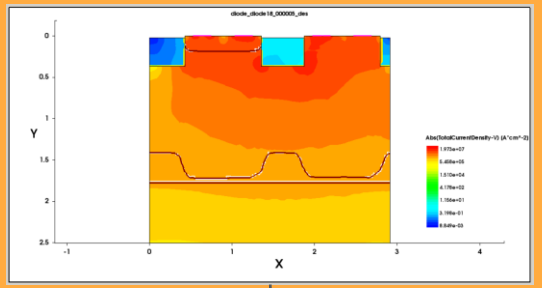
All of the factors followed the increased depth. The hotspot was pushed further down into the substrate.

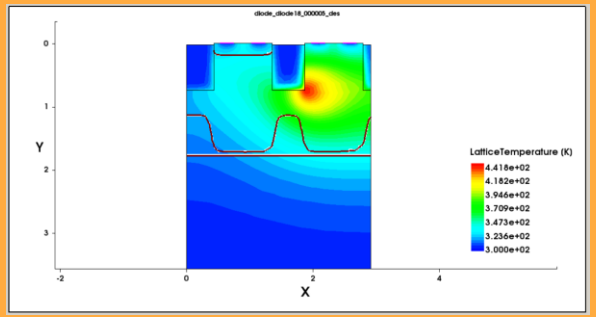
Higher temperatures now further in substrate, better for heat dissaption.

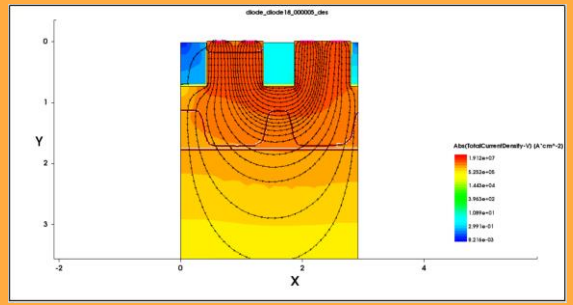
Changes with Depth

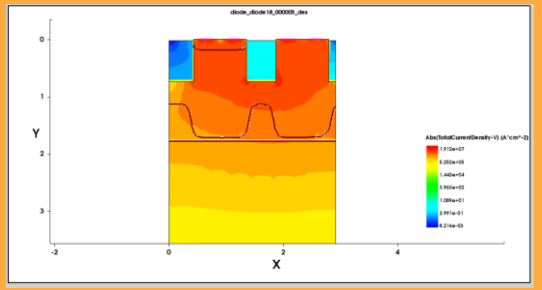




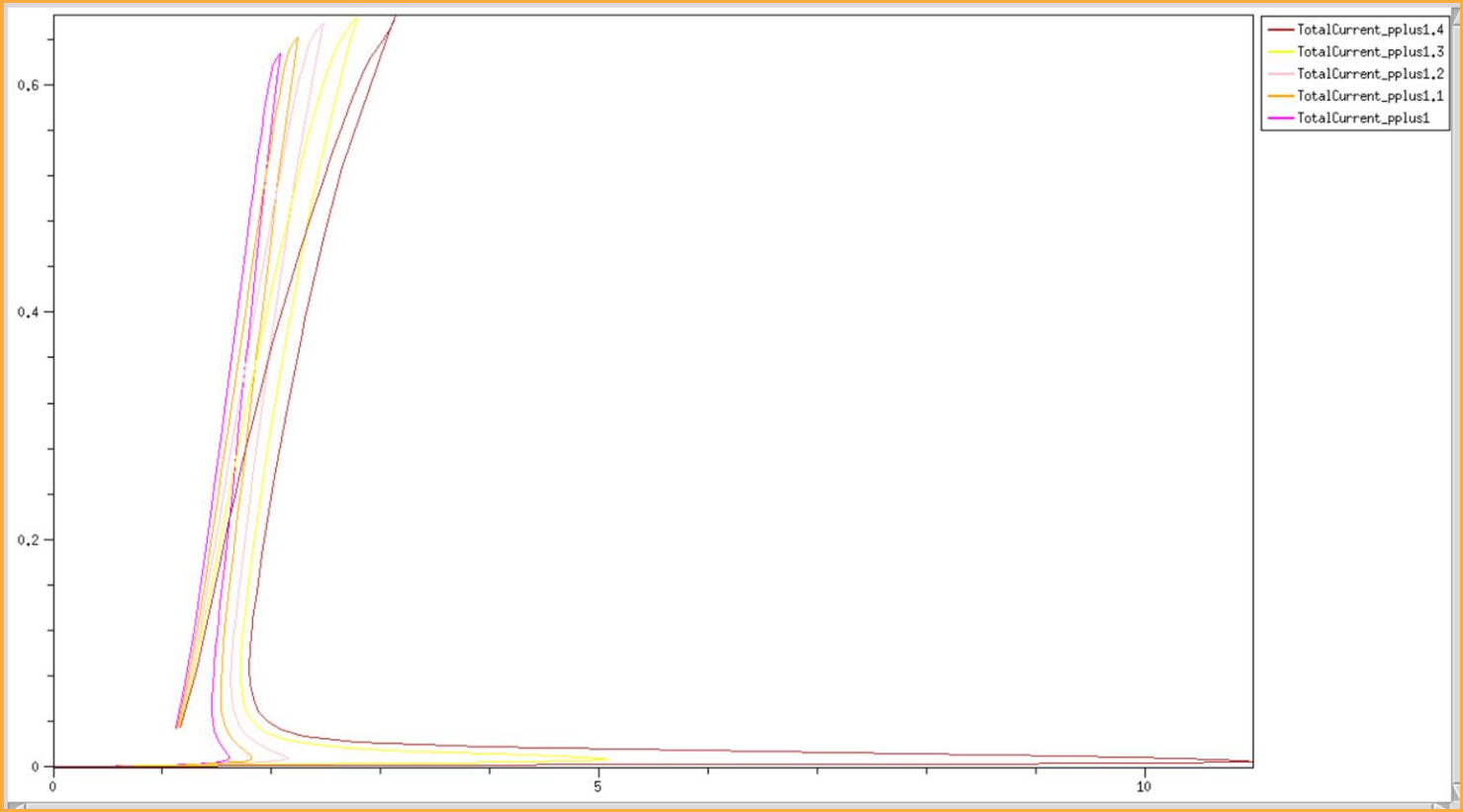




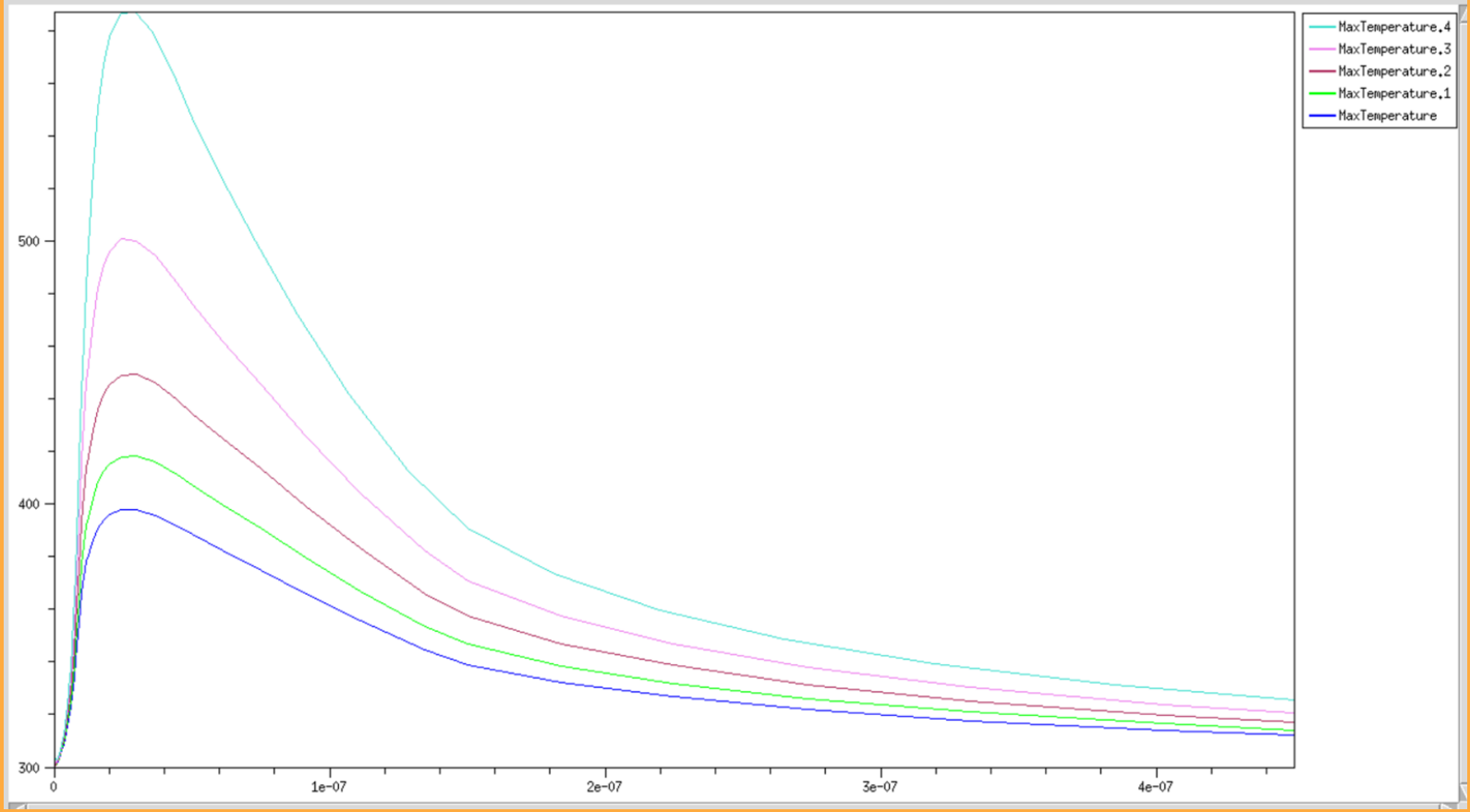




Depth Change: Total Current vs. Outervoltage



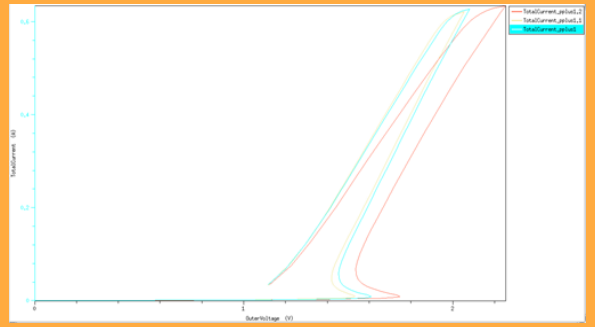
Depth Change: Tmax vs. Time

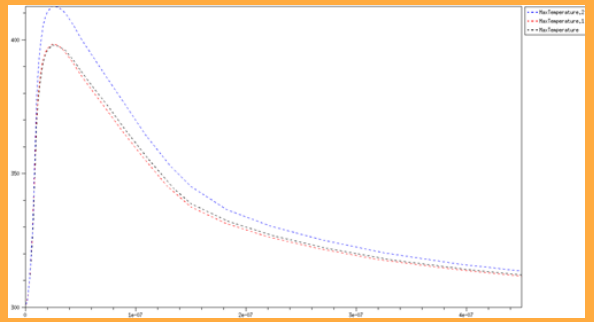


Manipulation of Width of STI

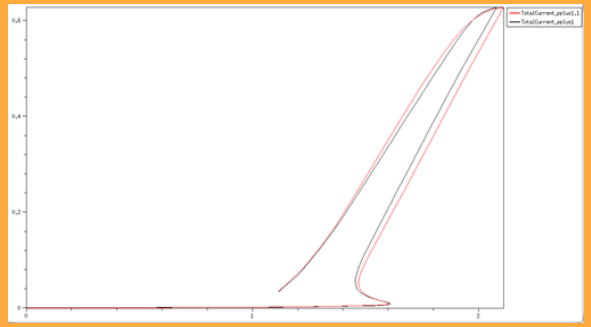
- Lattice Temperature
  - Better spread
  - Extremeties less hot
- Hotspots
  - Slightly right
- Current Streamlines
  - Larger area spread
- Tmax correlation
- Vt1 Correlation

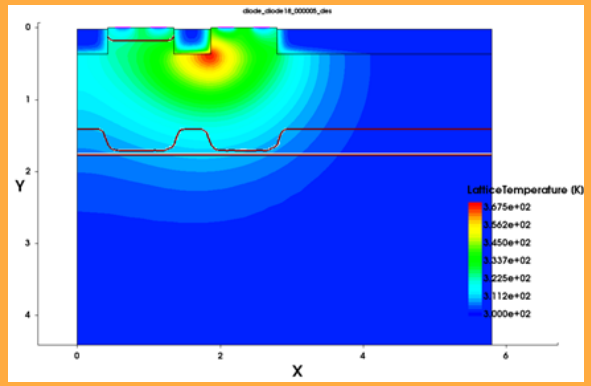
All of these factors were affected by STI width.





Change of STI Width on one side

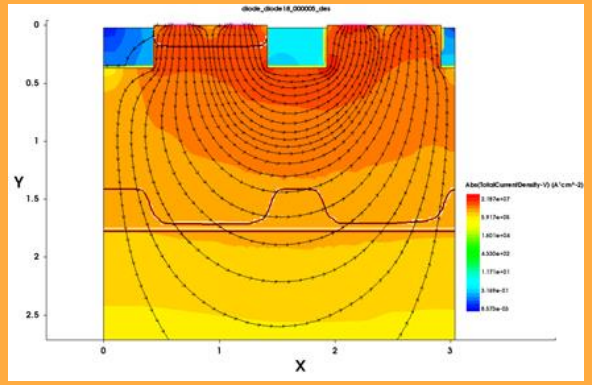


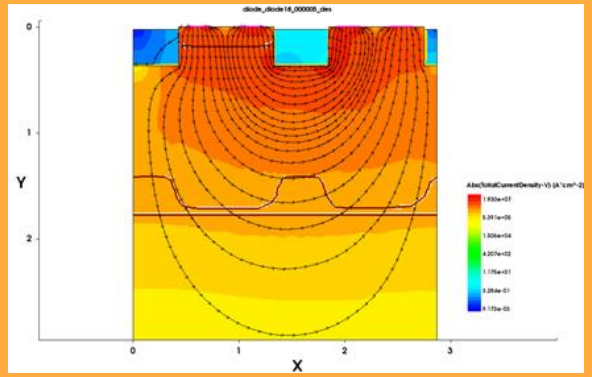


Width

- Lattice Temperature
  - Slightly lower Tmax
- Hotspots
  - No change in location, more spread out
- Current Streamlines
  - Spread slightly right
- No vt1 change

Change in Gap Width





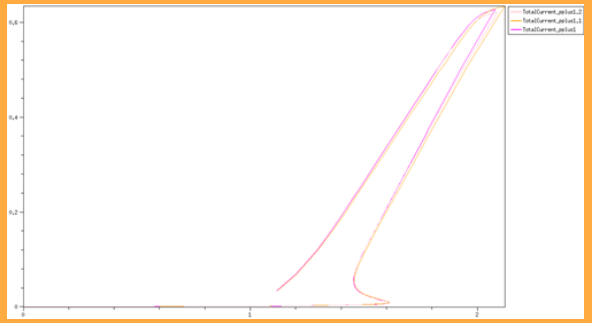
Width

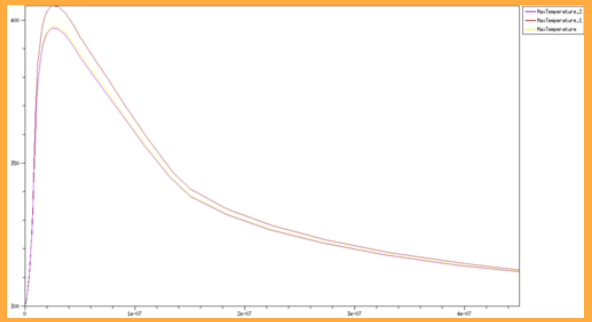
- Lattice Temperature
  - Better spread
  - Extremeties less hot
- Hotspots
  - No noticeable change
- Current Streamlines
  - Larger area spread
  - Better spread

Change in Width of N+&P+ Wells

Width

- Lattice Temperature
  - Better spread
  - Extremeties less hot
- Hotspots
  - No change
- Current Streamlines
  - No change
- Vt1 No change





Questions?

Design of Diode for Higher Voltage use cases through Manipulation of STI, gaps, and N+, P+ Diffusion Wells

I. Abstract

We present the optimization of a single Diode for Higher Voltage (~3.3V) through manipulation of STI depth/width, N+P+ width, as well as diffusion width manipulation.

II. Introduction

The diode is one of the most basic ESD protection circuits. When used appropriately it can and will provide useful ESD protection. However, a typical diode will turn on at ~1.6V-1.8V and while this may be fine for low voltage systems, it fails to be of use at higher voltages like at around ~3.3V.

In this paper, we provide analysis of the effects of STI depth and width on performance (i.e. Trigger-voltage and failure current) of a Diode and therefore the feasibility of STI manipulation to increase the use case for a Diode without increasing area size through Diode stringing.

III. Method

TCAD simulation was used to model the diode and subsequently test it using the HBM Model at 2kV.

IV. STI Depth Results

Image Set(s) 1-5 show the results of TCAD simulation results of a Diode, consisting of current density, current streamlines, and lattice temperature after simulation[1]. In reference to a base rate of ~0.3692, the rate was multiplied by a time factor ranging from 1s to 2s at 0.25 increments (for example [1.00s, 1.25s, 1.5s, 1.75s, 2.0s]). With increased depth everything was pushed down accordingly. As expected the current was forced deeper towards the substrate as well as the hotspot following the bottom-right corner of the substrate. The STI in general provides excellent isolation lessening leakage current.

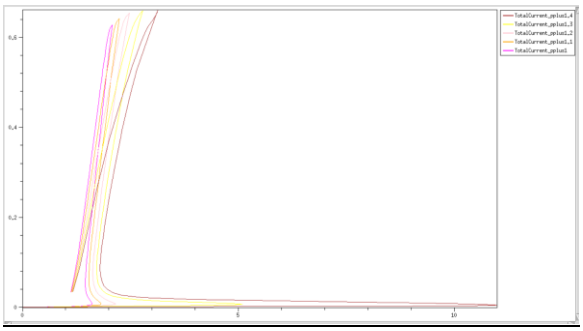


Fig 1

The trigger-voltage did not scale linearly, at first a difference in etching time scale of 0.25 make small increases in trigger-voltage until you get to a deeper trench which doubled the amount of time etching. The trigger voltage becomes very large, going past ~10V. But the snapback Vt2 is roughly in the same area which is nice. Another notable change is the Ron value, i.e. the slope after loses verticality with increasing STI/Trigger-voltage.

[1]Refer to appendix of images at the end. Any further mention of unseen figures, please see appendix.

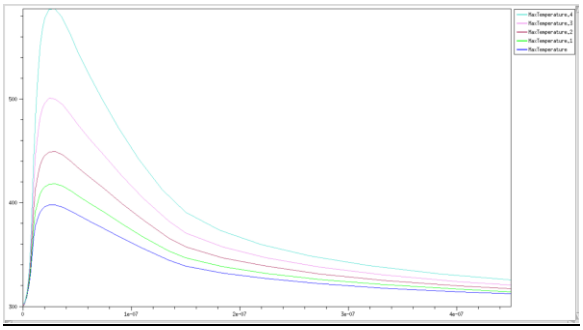


Fig 2

In the figure above we have Max Temperature vs Time, the lowest line is the baseline of time spent etching which corresponds to the shallowest trench. We see the STI with the greatest trench depth reached the highest T_{MAX} = ~600C. The max temperature scaled well with an increase in STI depth.

V. STI side increase Results

Image Set(s) 6-7 show the results of TCAD simulation results of a Diode, consisting of current density, current streamlines, and lattice temperature after simulation[1]. In reference to the base width of 0.12 of the right side STI, the width was set equal to the total length of the original structure. With increased width on the right side only, all other dimensions remained unchanged. As expected the current remained stronger on the left side of the structure, though current spread further to the right than in the original structure. A hotspot was located at the top left of the substrate, with the temperature being much higher on the left than he right. The STI in general provides better isolation and lessens leakage current but increases the difference in temperature throughout the structure dramatically.

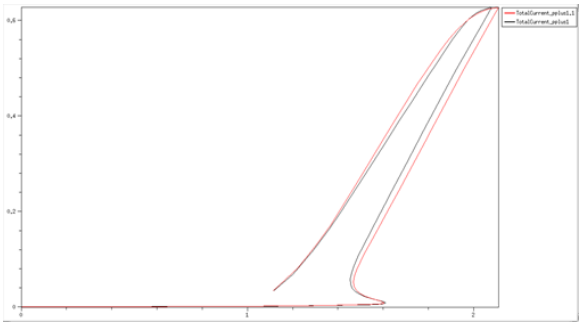


Fig 19

This figure displays Total current vs Outer voltage. The Black line is the unchanged file (control) and the orange is the new structure. The trigger-voltage Vt1 appears to be the same as the control file ~1.6V. The snapback Vt2 is roughly in the same area but happens slightly at slightly higher voltage. The Ron value appears to remain unchanged.

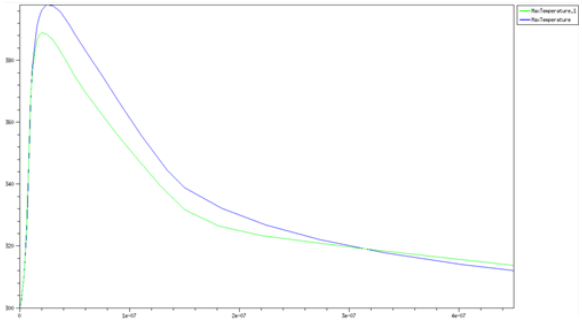


Fig 20

In the figure above we have Max Temperature vs Time, the highest line is the control while the lowest one is the one being tested with an increased right side STI width. We see the STI with the increased STI width reached a lower T_{MAX} = ~370C.

VI. Gap Width Results

Image Set(s) 8-10 show the results of TCAD simulation results of a Diode, consisting of total current density, the same figure with current streamlines, and lattice temperature after simulation[1]. In reference to the original file (control), provided by the lab 1 file, we compared the diode's efficiency when the gap width between each STI and N+ or STI and P+ is changed by a factor of 1.3 (tests both increase and decrease). There appears to be little impact on the size/location of the hotspots. However, Current is spread out more evenly and deeper when the gap is increased than the control, and less evenly and closer to the top when the gap is decreased compared to control.

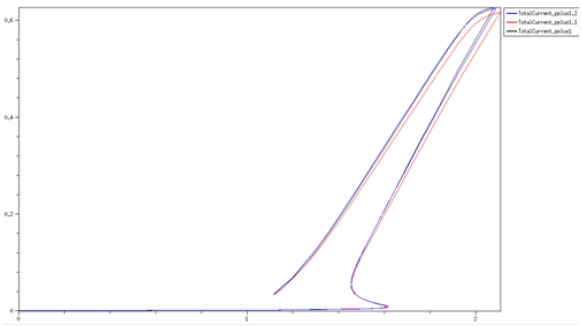


Fig 24

This figure displays Total current vs Outer voltage. Black is the control, red is the sample for decreased gap and blue for increased gap. The trigger-voltage Vt1 appears to be exactly the same for all three curves ~1.6V. It1 is also very similar.The snapback Vt2 is roughly in the same area which is nice. Voltage for Vt2 appears to correlate negatively with gap size while current It2 correlates positively. Th Ron value remains similar.

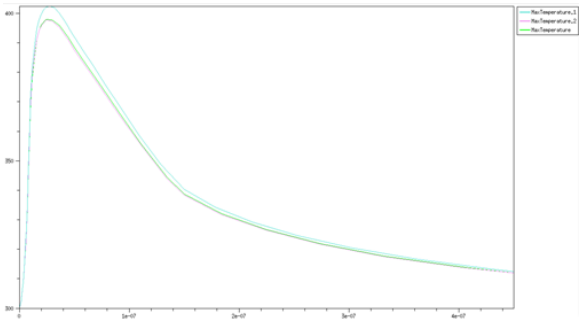


Fig 25

In the figure above we have Max Temperature vs Time. Green is the control, blue in decreased gap, and pink is increased gap. We see that a decrease in gap results in a higher (highest) T_{MAX} = ~410C. The max temperature did not scale linearly with an increase in STI depth as the difference between the increased gap and control simulation Tmax is very minimal though the trend stands true.

VII. N+, P+ Width Results

Image Set(s) 11-13 show the results of TCAD simulation results of a Diode, consisting of total current density, the same figure with current streamlines, and lattice temperature after simulation[1]. In reference to the base width provided by the lab 1 file, we compared the diode's efficiency when the N+ and P+ width was changed by a factor of 1.3 (tests both increase and decrease). The figures for current distribution and hotspot seem to indicate that higher width correlates with more even spread of both current and

heat, though the trend is very minimal.

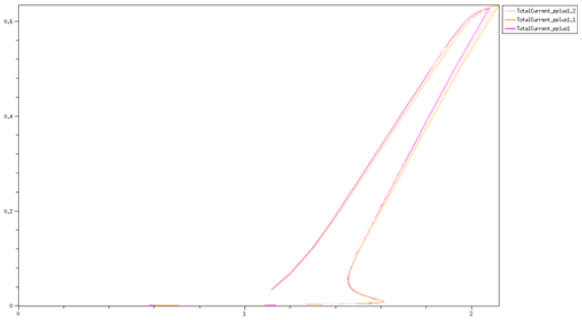


Fig 32

This figure displays Total current vs Outer voltage. The pink graph is the control, dark orange the decrease, and light orange the increase in N+, P+ width.The trigger-voltage Vt1 appeared unchanged with regards to these parameters at about 1.6V . The snapback Vt2 is roughly in the same area with the "Increase" and "Control" graphs showing little difference while the one displaying decreased width of N+, P+ displayed slightly higher Vt2 and lower It2. The Ron value is very similar across all three samples.

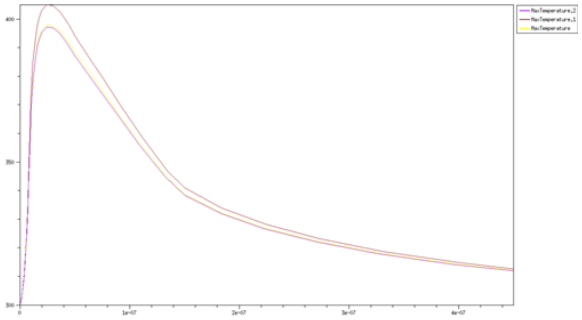


Fig 33

In the figure above we have Max Temperature vs Time Yellow represents the control, purple the increase in N+, P+ width the decrease in this parameter. There is virtually no difference in Tmax between the "Increase" and "Control" lines but Tmax is higher by ~15C on the "decrease" line.

VIII. STI Width Results

Image Set(s) 14-16 show the results of TCAD simulation results of a Diode, consisting of total current density, the same figure with current streamlines, and lattice temperature after simulation[1]. In reference to the base width provided by the lab 1 file, we compared the diode's efficiency when the STI width changed by a factor of 1.3 (tests both increase and decrease). Current density spread was more even with the larger STI width and the hotspot was shift slightly right overall. The extremities of the structure had lower temperature as STI width increased.

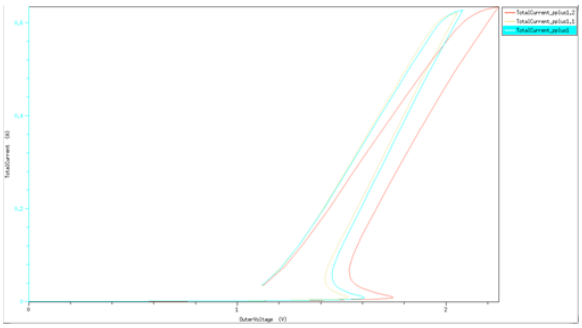


Fig 40

This figure displays Total current vs Outer voltage. The yellow curve is the decrease in STI width, the blue one the control and the red one the increase in that parameter. The trigger-voltage did not scale linearly increased with increased STI width. It1 remained unchanged with regards to this parameter. The snapback Vt2 increases at STI width increases while It2 remains constant across the three curves. Ron

values is affected by STI width in the same way as it is affected by STI depth.

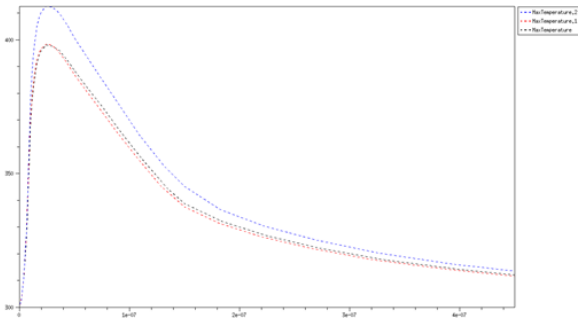


Fig 41

In the figure above we have Max Temperature vs Time. The red curve is the decrease in STI width, the black one the control and the blue one the increase in that parameter. While there appears to be little difference between the "control" and "Increased STI width curve", there is a significant increase in Tmax in the "Decreased STI width curve" of about 25C.

IX. Discussion

Regarding STI depth, at a rate of ~0.3692 multiplied by time between [1.5, 1.75] would produce the desired result of a ~3.3V trigger-voltage. Further testing is required to fine tune the timing that will produce an STI depth that gives the desired Vt1. STI width does not affect trigger voltage if only one of the left/right most STI width is changed. However, there is a positive correlation between STI width and Vt1 when all three STI are changed by the same factor. This suggests that the width of the middle STI has more of an effect on Vt1 than the extremity ones. The effect of STI width on Vt1 is not as dramatic as that of STI depth. This could allow for further fine tuning of triggering voltage. The STI width increase by a factor of 1.3 should be preferred due to the lower Tmax and higher Vt1, which allows for STI depth to not be as large (though still within t=1.5-t=1.75). Depth N+ and P+ width did not appear to affect triggering voltage. Considering that factors such as Tmax were either worse or the same as the control, N+ and P+ width should remain the same as that of the control. gap width did not have a significant impact on triggering voltage but made other factors better. The increase of gap by a factor of 1.3 should be used as it decreased Tmax and had a more even spread of both lattice temperature and current in the structure.

X. Conclusion

It is a feasible option to manipulate the STI depth to increase the trigger-voltage of the singular Diode to handle higher voltages. The scaling of the trigger-voltage was good and the ability to manipulate it is within reason. Further testing would be required to see if there are unknown detrimental effects to performance. But one known problem is the current crowding around the edges of the STI which lead to hotspots at one corner.

Changing the width of the STI and and Diffusion layers had a minor impact on the trigger-voltage but not enough to warrant as a method to optimize the diode for higher voltages. It did have minor improvements in temperature and spreading of current compared to the original design.

XI. Appendix

Image Set 1:

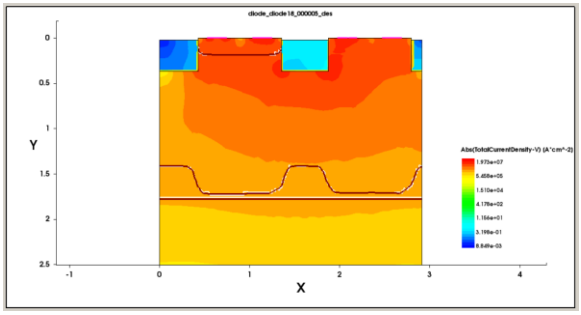


Fig 3

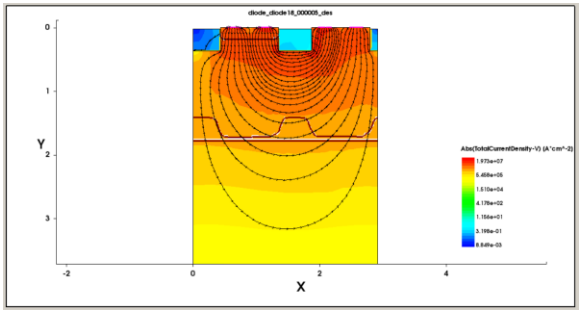


Fig 4

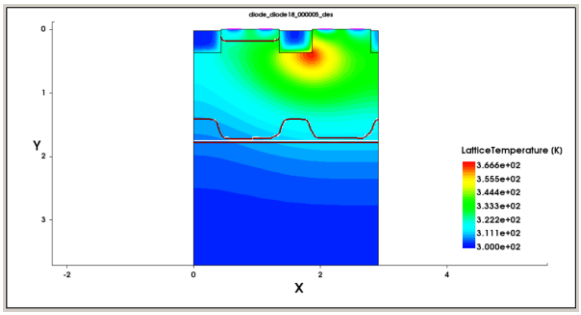


Fig 5

Image Set 2:

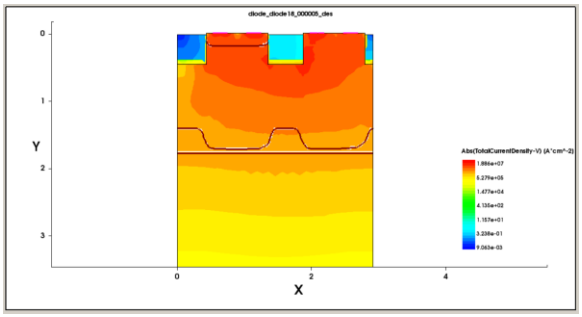


Fig 6

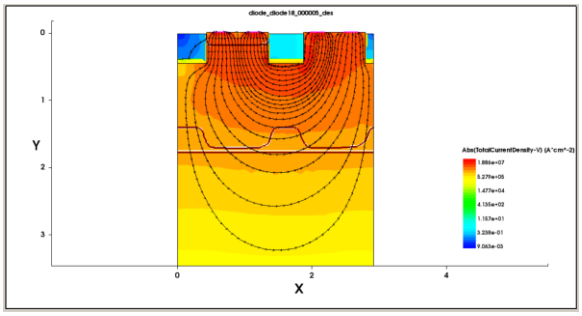


Fig 7

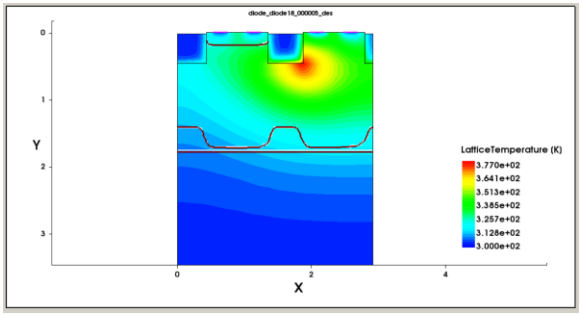


Fig 8

Image Set 3:

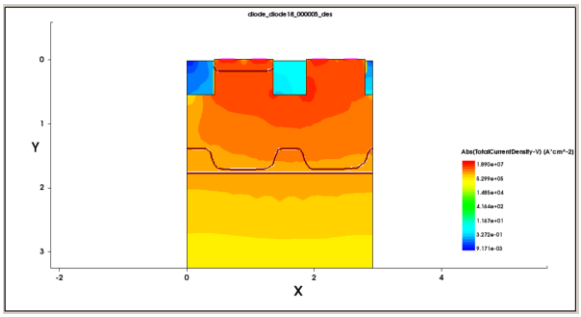


Fig 9

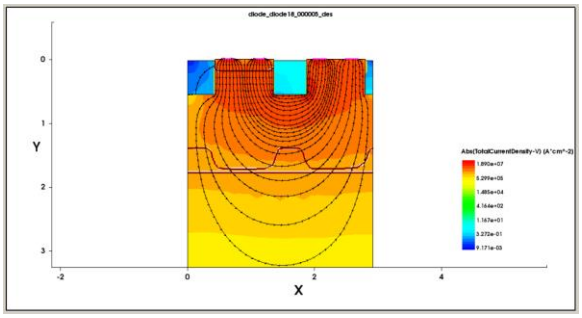


Fig 10

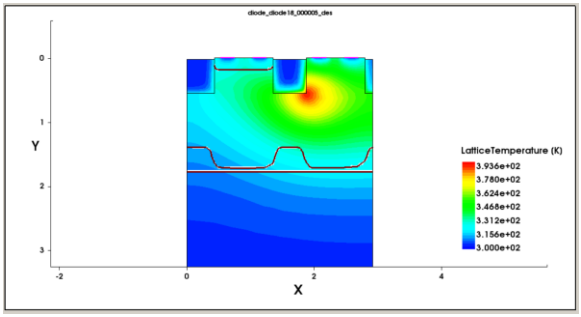


Fig 11

Image Set 4:

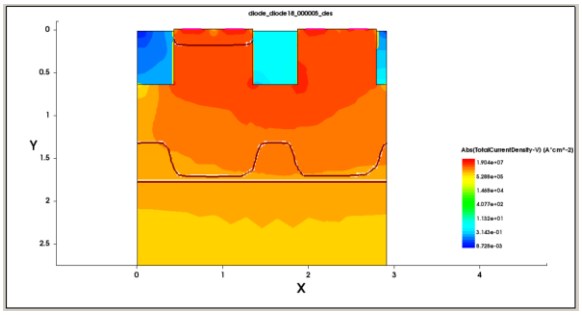


Fig 12

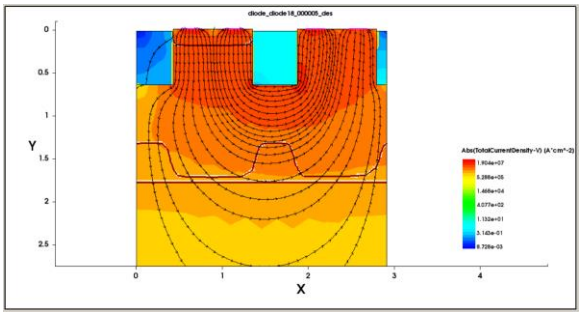


Fig 14

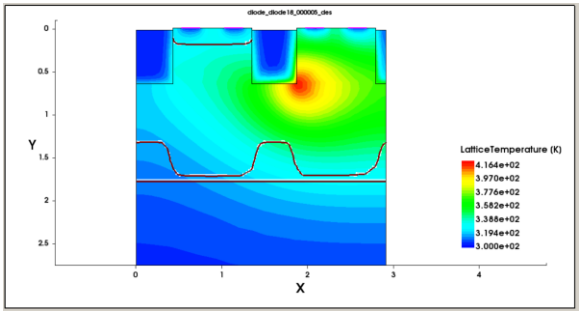


Fig 15

Image Set 5:

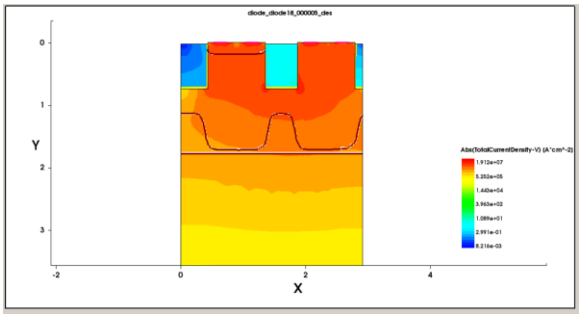


Fig 16

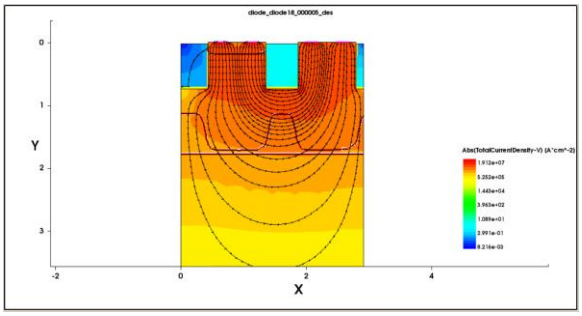


Fig 17

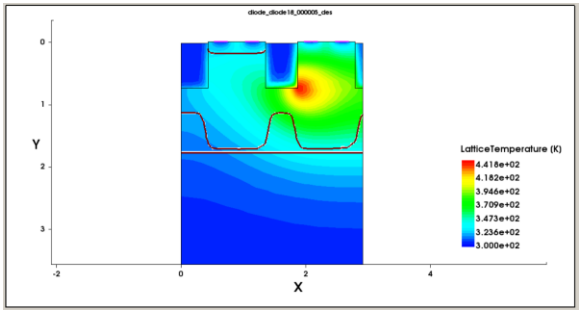


Fig 18

Image Set 6: (shift left)

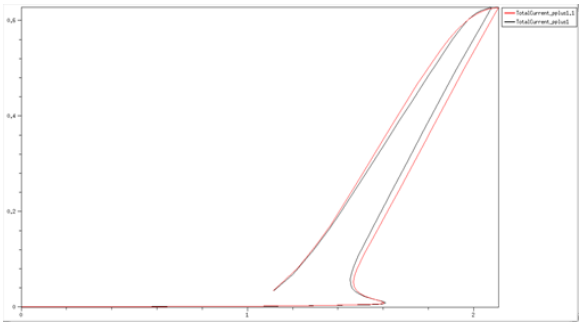


Fig 19

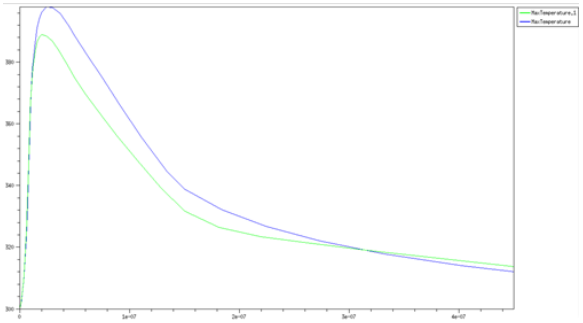


Fig 20

Image Set 7: Shift left pt2

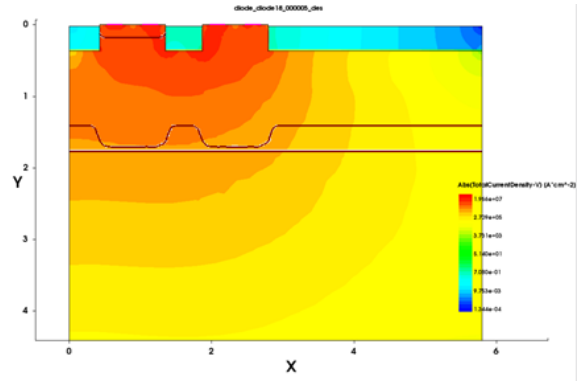


Fig 21

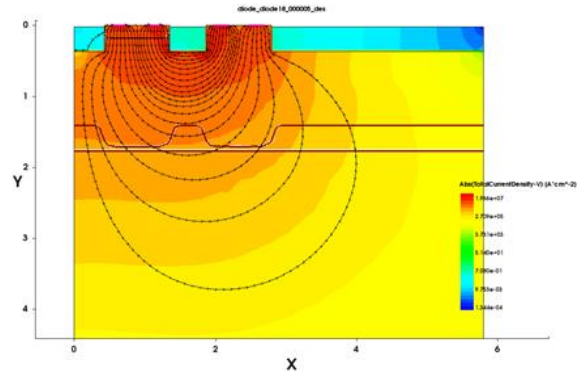


Fig 22

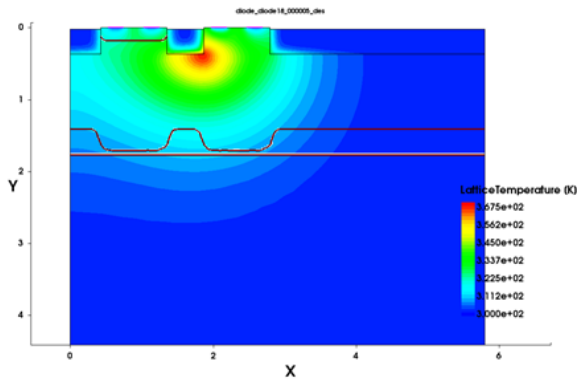


Fig 23

Image Set 8: Trench Width

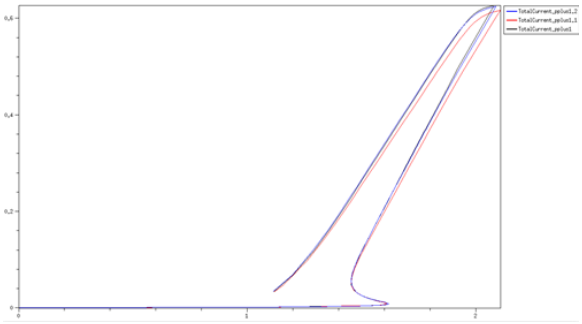


Fig 24

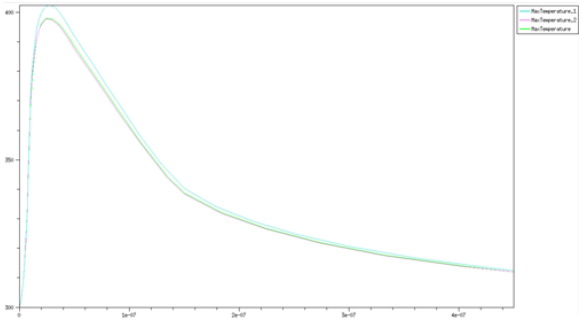


Fig 25

Image Set 9: Gap width divided by 1.3 factor

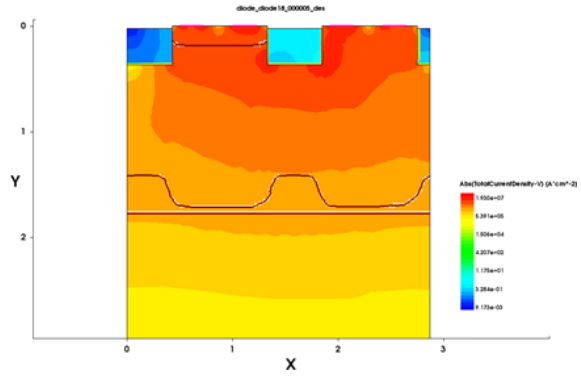


Fig 26

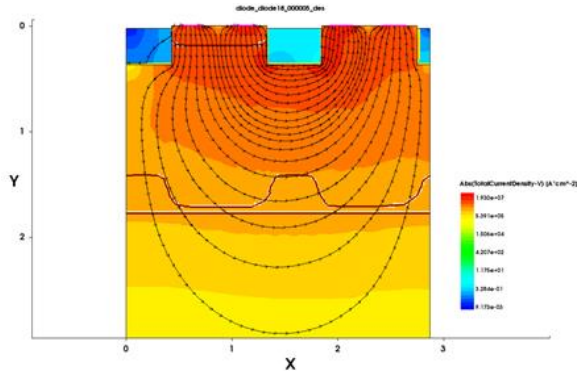


Fig 27

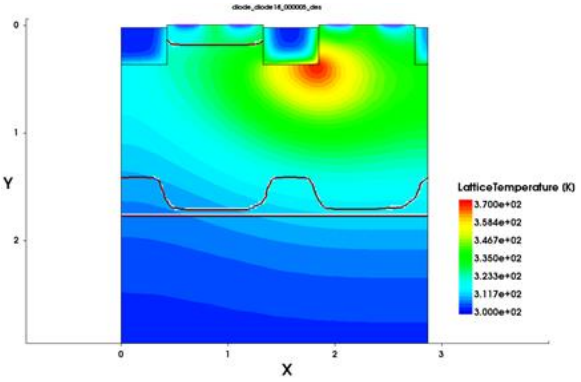


Fig 28

Image Set 10: Gap width multiplied by 1.3 factor

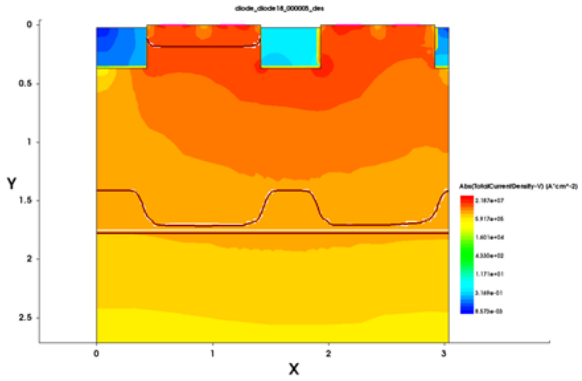


Fig 29

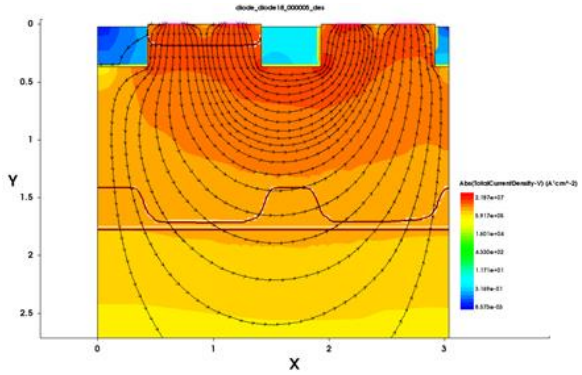


Fig 30

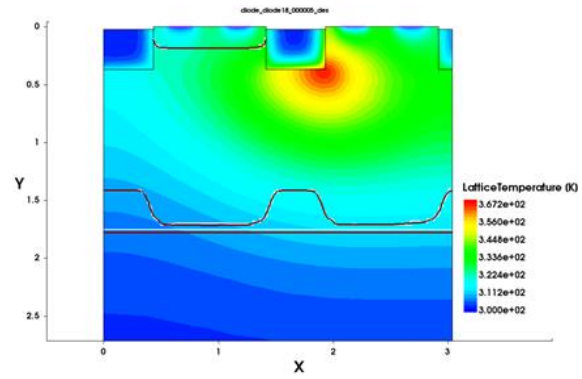


Fig 31

Image Set 11: N+, P+ wells width change

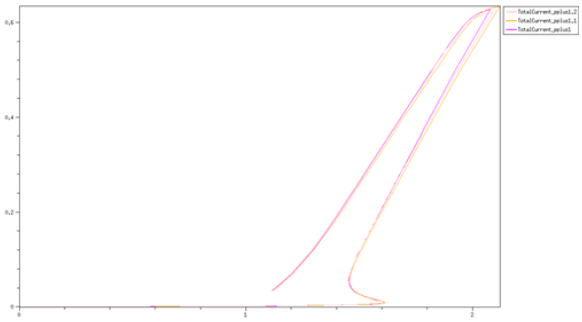


Fig 32

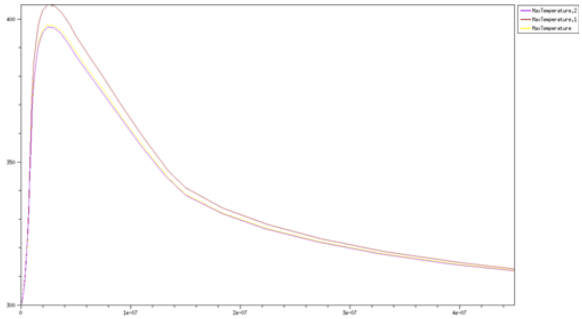


Fig 33

Image Set 12: N+P+ width divided by factor of 1.3

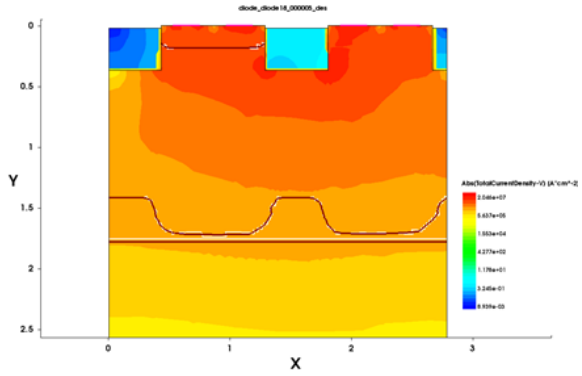


Fig 34

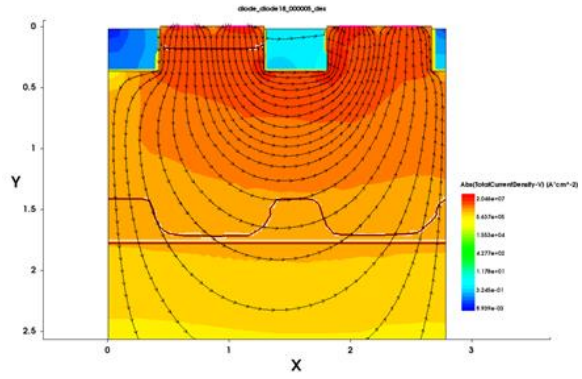


Fig 35

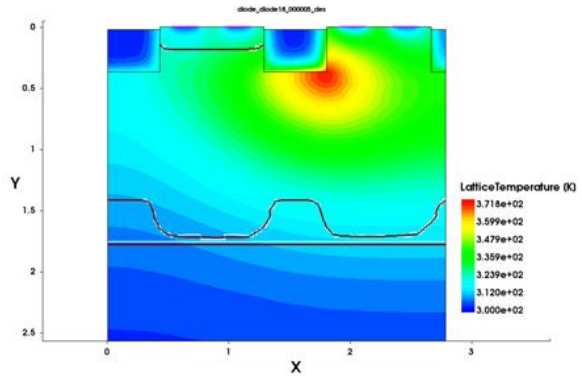


Fig 36

Image Set 13: N+P+ width multiplied by factor of 1.3

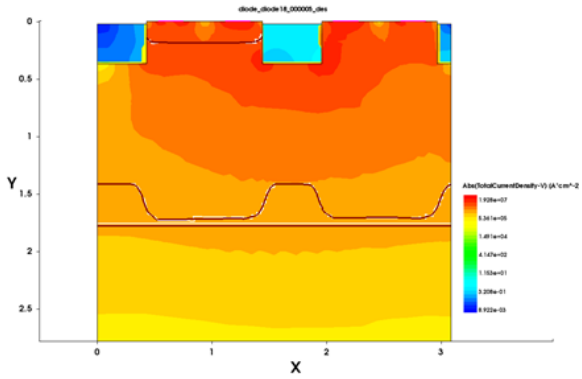


Fig 37

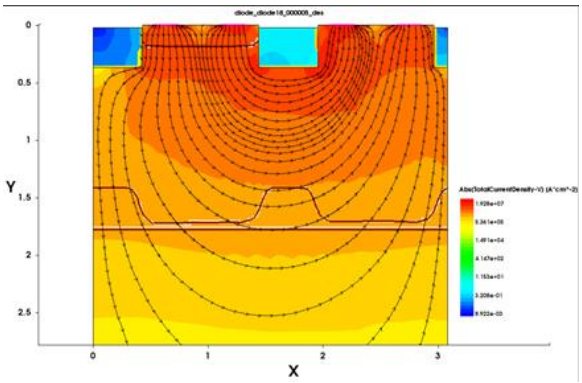


Fig 38

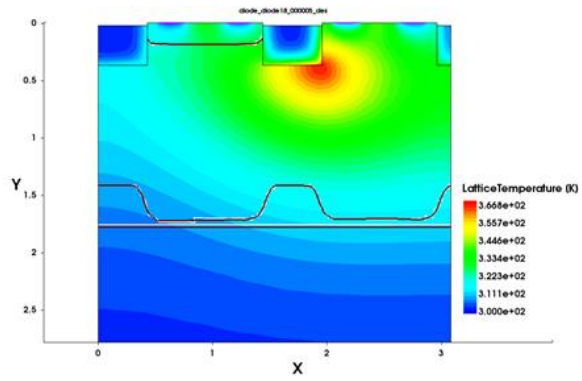


Fig 39

Image Set 14: STI width

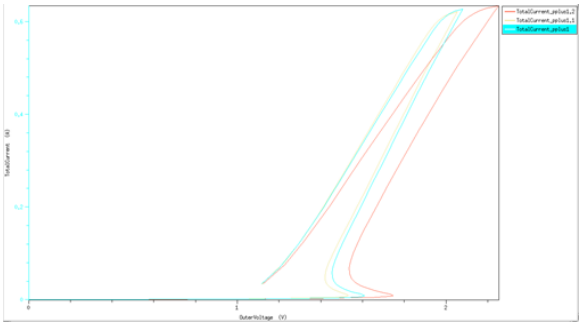


Fig 40

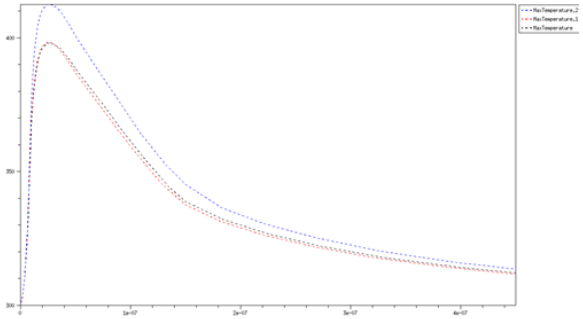


Fig 41

Image Set 15: STI width divided by factor of 1.3

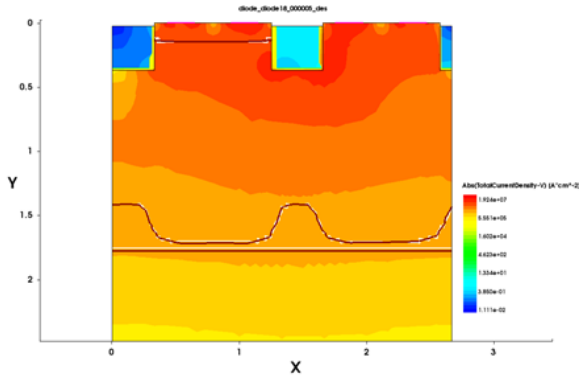


Fig 42

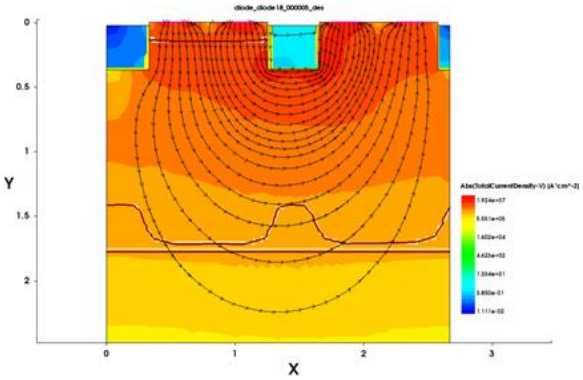


Fig 43

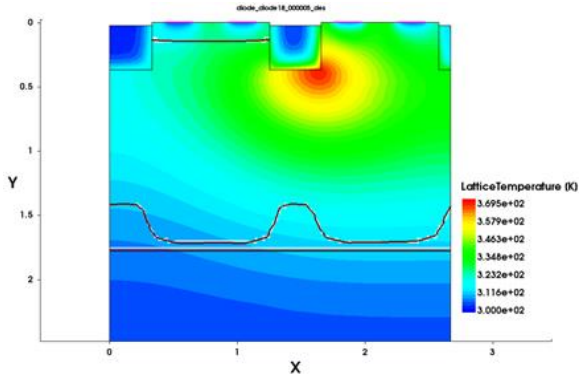


Fig 44

Image Set 16: STI width multiplied by factor of 1.3

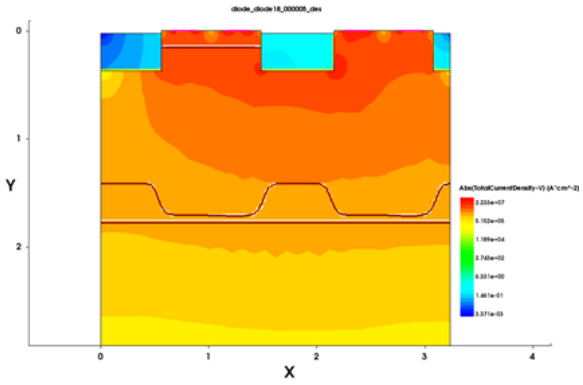


Fig 45

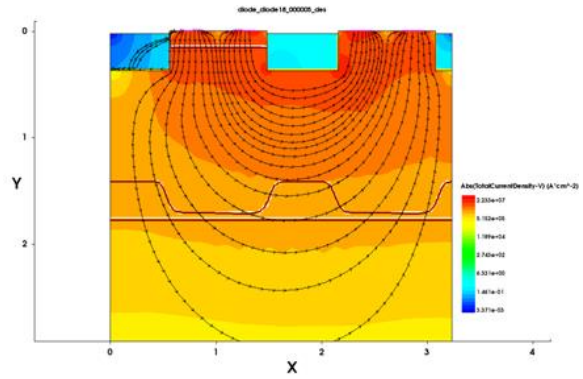


Fig 46

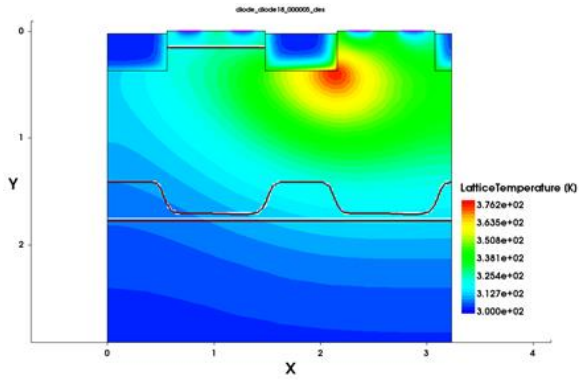


Fig 47